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| A7D18627  **COMSATS UNIVERSITY ISLAMABAD,**  **ATTOCK CAMPUS** |

**ASSIGNMENT #01**

**Digital System Design**

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| Program | BCE |
| Semester | VII |

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**2 Bit Comparator:**

* **Verilog Module**

module Com2Bit(AgB, AlB, AeqB, A, B);

input [1:0]A, B;

output AgB, AlB, AeqB;

wire A0n, A1n, B0n, B1n;

wire AgBw1, AgBw2, AgBw3;

wire AlBw1, AlBw2, AlBw3;

wire AeBw1, AeBw2, AeBw3, AeBw4;

not(Aon, A[0]);

not(A1n, A[1]);

not(Bon, B[0]);

not(B1n, B[1]);

and A1(AgBw1, A[1], B1n), A2(AgBw2, A[1], A[0],Bon), A3(AgBw3, A[0], B1n, Bon), A4(AlBw1, A1n, Aon, B[0]), A5(AlBw2, Aon, B[1], B[0]), A6(AlBw3, A1n, B[1]), A7(AeBw1, Aon, A1n, Bon, B1n), A8(AeBw2, A[0], A[1], B[0], B[1]), A9(AeBw3, A[1], Aon, B[1], Bon), A10(AeBw4, A1n, A[0], B[0], B1n);

or O1(AgB, AgBw1, AgBw2, AgBw3), O2(AlB, AlBw1, AlBw2, AlBw3), O3(AeqB, AeBw1, AeBw2, AeBw3, AeBw4);

endmodule

* **RTL Schematic:**

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| Figure : 2 Bit Comparator | Figure : Detailed Diagram of 2 Bit Comparator |

**4-bit Comparator Using 2 Bit Comparator:**

* **Verilog Module Code:**

module Com4BitUsing2BitCom(AgB, AlB, AeqB, A, B);

input [3:0]A, B;

output AgB, AlB, AeqB;

wire AgB1w, AlB1w, AeqB1w;

wire AgB2w, AlB2w, AeqB2w;

wire w1, w2;

Com2Bit Com2Bit1(AgB1w, AlB1w, AeqB1w, A[1:0], B[1:0]), Com2Bit2(AgB2w, AlB2w, AeqB2w, A[3:2], B[3:2]);

and AgBA1(w1, AeqB1w, AgB2w), AgBA2(w2, AeqB1w, AlB2w), AgBA3(AeqB, AeqB1w, AeqB2w);

or AgBo1(AgB, w1, AgB1w), AgB02(AlB, w2, AlB1w);

endmodule

* **RTL Schematic:**

**Diagram

Description automatically generated**

Figure : 4 Bit Comparator

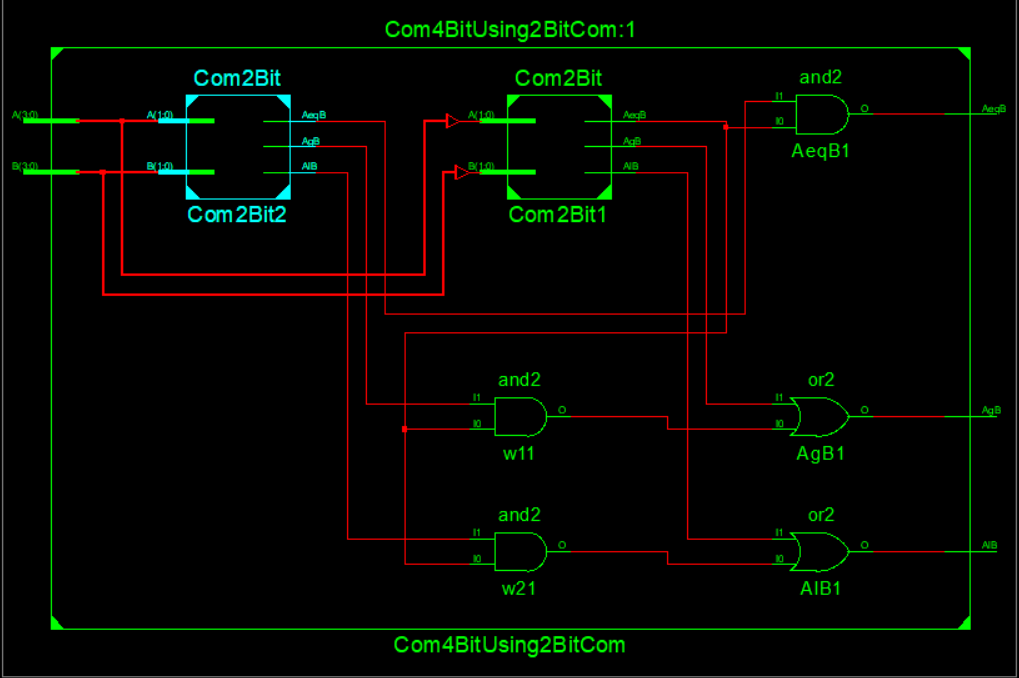
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Figure : 4 Bit Comparator Using 2 Bit Comparator.

* **Verilog Test Module:**

module BbitComTest;

// Inputs

reg [3:0] A;

reg [3:0] B;

// Outputs

wire AgB;

wire AlB;

wire AeqB;

// Instantiate the Unit Under Test (UUT)

Com4BitUsing2BitCom uut (

.AgB(AgB),

.AlB(AlB),

.AeqB(AeqB),

.A(A),

.B(B)

);

initial begin

// Initialize Inputs

A = 4'b0000;

B = 4'b0000;

// Wait 100 ns for global reset to finish

#100;

// Add stimulus here

// Initialize Inputs

A = 4'b1111;

B = 4'b1010;

// Wait 100 ns for global reset to finish

#100;

// Add stimulus here

// Initialize Inputs

A = 4'b0010;

B = 4'b0111;

// Wait 100 ns for global reset to finish

// Add stimulus here

end

endmodule

* **Waveform Diagram**

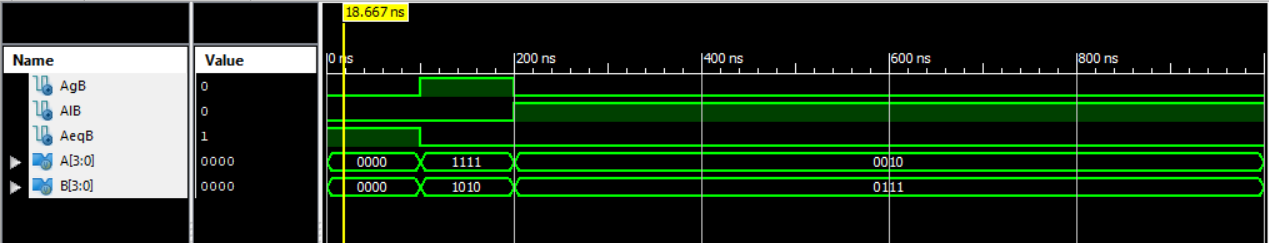


Figure : As you can see A's input is equal to the B's input that's why AeqB is equal to 1

Graphical user interface

Description automatically generated

Figure : As you can see, A's input is greater than B's input, that's why AgB is showing 1 on its box

Graphical user interface, diagram

Description automatically generated

Figure : As A's input is less than B's input that's why our AlB output is high (1).

Output of the waveform is showing the right results, We have matched these results with truth table too and it prove that this code is working fine.

